In the Claims:

1. A self-aligned contact structure comprising:

a plurality of spaced apart gate electrodes disposed on a semiconductor substrate with the gate electrodes having opposing first and second sidewalls and top and bottom surfaces, wherein adjacent sidewalls of selected neighboring gate electrodes have respective upper portions that angle toward each other to present a sloped profile;

a first liner layer that is disposed on the semiconductor substrate and covers one of the first and second sidewalls, a minor portion of the other sidewall and a major portion of the top surface of the gate electrodes;

a plurality of self-aligned contact pads that are separately electrically connected to selected regions of the semiconductor substrate, each self-aligned contact pad having opposing upwardly extending sidewalls, wherein a respective self-aligned contact pad is positioned between the selected neighboring gate electrodes , and have a length sufficient so that the self-aligned contact pads extend a distance above the top surface of the gate electrodes;

an interlayer insulation layer disposed on the first liner layer above the top surface and about selected sidewalls of respective gate electrodes, the selected sidewalls of respective gate electrodes being those sidewalls that are positioned away from the self-aligned contact pad electrodes; and

a second liner layer disposed on the angled portions of the adjacent sidewalls of neighboring gate electrodes.

2. The device of claim 1, wherein the gate electrodes are configured so that the second liner layer extends in a generally downward direction in a self-aligned contact window that holds the self aligned contact pad and is configured to extend above the top surfaces of the gate electrodes and down to an impurity diffusion region in the semiconductor substrate.

3. The device of claim 1, wherein the first liner layer has a thickness that is substantially the same over the gate electrodes.

4. The device of claim 1, further comprising a buffer insulation layer positioned proximate an upper portion of respective self-aligned contact pads between the second liner layer and sidewalls of the self aligned contact pad.

5. The device of claim 1, wherein the first and second liner layers comprise silicon nitride and the interlayer insulation layer comprises silicon oxide.

6. The device of claim 4, wherein the first and the second liner layers comprise silicon nitride, and the interlayer insulation layer and the buffer insulation layer comprise silicon oxide.

7. The device of claim 6, wherein the interlayer insulation layer comprises silicon oxide layer and the buffer insulation layer comprises silicon oxide that surrounds an upper portion of the self-aligned contact pad and terminates a distance above the semiconductor substrate.

Claims 8-26 (canceled).

27. An integrated circuit assembly, comprising:

a plurality of gate electrodes disposed on a substrate, the gate electrodes having opposing sidewalls and top and bottom surfaces, wherein portions of selected adjacent sidewalls of neighboring electrodes angle generally downwardly and inwardly toward each other while the opposing sidewall of each of the selected sidewalls are substantially linear.

28. An assembly according to claim 27, further comprising;

a plurality of elongate contact windows, a respective one positioned between the selected sidewalls of neighboring electrodes, wherein the contact window sidewalls comprise an angled profile that correspond to the angled gate electrode sidewall configuration; and

a contact pad disposed in each contact window, the contact pad extending generally downwardly and having a length that is greater than the height of the gate electrodes.

29. An assembly according to claim 28, further comprising:

a gate protection liner layer that extends in the contact window and covers the angled sidewall portion of a respective gate electrode; and

a first liner layer that covers the remaining surfaces of the top and opposing sidewalls of the respective gate electrode.

30. An assembly according to claim 29, wherein the angled sidewall is configured on the second sidewall of a first gate electrode and on the first sidewall of the adjacent sidewall of the neighboring second electrode, wherein the first sidewall of the first gate electrode and the second sidewall of the second electrode are generally vertical, wherein the first liner layer covers: (a) greater than a major portion of the top surface of both the first and second gate electrodes; (b) a minor portion of the second sidewall of the first gate electrode and minor portion of the first sidewall of the second gate electrode; and (c) the entire length of the first sidewall of the first electrode and the second sidewall of the second electrode.

31. An assembly according to Claim 29, wherein the bottom surface of the gate electrodes contact the semiconductor substrate, and wherein the remaining external surfaces are covered by at least one of the first and second liner layers so that the gate electrodes are encased.

32. A semiconductor assembly with self-aligned contact pads, comprising:
a cell array region comprising:

first and second gate electrodes disposed on a semiconductor substrate, the first and gate electrodes having opposing first and second sidewalls and top and bottom surfaces, wherein portions of the adjacent sidewalls of the first and second gate electrodes are configured to angle generally downwardly and inwardly toward each other;

a contact window positioned between the adjacent sidewalls of the first and second gate electrodes, wherein the contact window sidewalls comprise an angled profile that correspond to the angled gate electrode sidewalls; and

a contact pad disposed in the contact window, the contact pad extending generally downwardly and having a length that is greater than the height of the gate electrode;

and a peripheral circuit region disposed on the semiconductor substrate spaced apart from the cell array region, the peripheral circuit region comprising:

at least one gate electrode;

lightly doped impurity diffusion regions in the semiconductor substrate positioned on opposing sides of the at least one gate electrode; and

heavily doped impurity diffusion regions in the semiconductor substrate positioned on opposing sides of the at least one gate electrode so that the heavily doped impurity diffusion regions reside a further distance away from the at least one gate electrode and so that the heavily doped impurity diffusion regions abut the lightly doped impurity diffusion regions.

33. An assembly according to claim 32, further comprising:

a gate protection liner layer that extends along the sidewalls of the contact window and covers the angled sidewall portion of a respective gate electrode in the cell array region; and

a first liner layer that covers target surfaces of the gate electrodes disposed in the cell array region and/or the peripheral circuit region.

34. An assembly according to claim 33, further comprising a buffer insulation layer disposed in an upper and/or intermediate portion of the contact window intermediate the contact pad and the gate protection liner layer.

35. A semiconductor assembly, comprising:

a conductive contact on a substrate in a recess adjacent to a gate electrode having an opposing top and bottom and a gate electrode sidewall that extends from a top surface to the bottom of the sidewall, the gate electrode sidewall angling inwardly from the top surface to an intermediate portion of the sidewall toward the recess with a lower portion of the sidewall being substantially straight so that the bottom of the electrode has a greater width than the top, the conductive contact having a profile that includes the angled shape of the gate electrode sidewall and an upper portion that extends above the top surface of the gate electrode.

Claim 36 (canceled).